DR. R SOLOMON ROACH

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LANGUAGES

English

Tamil

SKILLS

Project Management

Team setting

Training the engineers in VLSI Domain

DfT Implementation

ATPG & SCAN insertion

MBIST insertion

Team Handling

PROFILE

Experienced professional with 5 years in industry and 14 years in academic, specializing in the field of VLSI design/Design for Testability (DfT). Demonstrated ability to bridge academic theories with practical applications, enhancing student learning through real-world examples and research-driven insights. Proven track record in leading projects, developing innovative solutions, and delivering high-quality education. Seeking to leverage both teaching and industrial expertise to contribute to academic and research goals.

Experienced professional with 5 years in the industry and 14 years in academia, specializing in VLSI design and Design for Testability (DfT). I aim to leverage my extensive expertise in integrating theoretical concepts with practical applications to advance research and enhance educational programs. My goal is to drive innovation and excellence in VLSI design by combining real-world experience with academic insights, thereby contributing to both scholarly advancement and practical solutions.

EDUCATION HISTORY

- **PhD** (VLSI Design), Anna University-Chennai, Tamil Nadu, India. Year -2018.
- **M.Tech** (VLSI Design), Bharath Institute of Higher Education and Research, Chennai, Tamil Nadu, India. Year -2005.

Paper publications in Journals & Conferences

Delivered Technical session for P.G & U.G graduates

Handled projects in PhD, P.G & U.G level.

INTERESTS

- Design for Testability (DfT)
- Memory BIST (MBIST)
- Embedded Deterministic scan Test (EDT)
- VLSI System Design
- Streaming Scan Network (SSN)
- Low Power VLSI Design
- Digital Signal Processing IC
- Embedded System
- Digital Electronics
- Microprocessor and Microcontroller
- Computer Architecture

MEMBERSHIP DETAIL

- Member of IEEE.
- Life Member of ISTE.

REFERENCE

Dr. D. NIRMAL

Professor & Head of the Department, Electronics

- **B.E** (Electrical & Electronics Engineering), St. Xavier's Catholic College of Engineering, Chunkankadai, Manonmaniam Sundaranar university, Tamil Nadu, India. Year-2002.

WORK EXPERIENCE

- **Operational** Manager in MEL Research & Advanced Development center, Nagercoil, Tamil Nadu, India from March 2025 to till date.
- **Manager Design Engineering** in the DfT division, Tessolve Semiconductor pvt Ltd, Bangalore, India from April 2023 to Jan 2025.
- **Senior Design Lead Engineer** in the DfT division, Tessolve Semiconductor pvt Ltd, Bangalore, India from Jan 2020 to March 2023.
- **ASIC Design Engineer** in the DfT division, Test and Verification Solutions Ltd, Chennai, India from June 2019 to Jan 2020.
- **Design Lead,** Vals Technology, Nagercoil, Tamil Nadu, India from July 2018 to June 2019.
- **Head of the Department** in the Department of Electronics and Communication Engineering, Cape Institute of Technology, Tirunelveli, Tamil Nadu, India from June 2017 to July 2018.
- **Assistant Professor** in the Department of Electronics and Communication Engineering, Cape Institute of Technology, Tirunelveli, Tamil Nadu, India from January 2010 to May 2017.
- **Lecturer** in the Department of Electronics and Communication Engineering, Francis Xavier Engineering College, Tirunelveli, Tamil Nadu, India from September 2006 to December 2009.
- **Design Engineer,** Vals Technology, Nagercoil, Tamil Nadu,

and Communication Engineering, Karunya Institute of Technology and Sciences (Deemed to be University), Coimbatore, India - 641114.
Mobile: +919789498810
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- Dr. D Ramji
  Design Lead DfT
  Tessolve Semiconductor Pvt ltd, Bangalure.
  India.
  Mobile:+91 9790540004
  Email: ramjidr@gmail.com

India from July 2005 to September 2006.

PROJECT HANDLED

1. **Project Name: Kking (Alphawave IP)**

   A high-speed communication chip for networking, AI & 5G. The soc with 238 memory instants with 15 controllers. With 5 clock domains of maximum frequency of 830 Mhz.

   Task Competed:

   - DfT Implementation
   - Spyglass
   - LEC
   - MBIST insertion
   - Pattern generation
   - RTL simulation & GLS simulation

2. **Project Name: GNRRO (INTEL)**

   A Server Soc have 256 partitions. 30 clock domains. The SSN DfT architecture used in the design. The EDT is used for each partition.

   Task Completed:

   - ATPG for stuck-at & AT speed Test.
   - STA Analysis
   - Simulation & Debug on Chain, Clk_cap, Hvm1, Hvm2 & Hvm3 patterns for Stuck-at & AT-speed patterns.

3. **Project Name: DIG-ABDT (Analog Devices)**

   A mixed signal SoC have 2 partitions. Clock domains used 10, technology node 22nm. Total FF count ~250K.

   - The dft architecture of the SoC comprises of

implementing XOR compressor wrappers and OPCG.

- MAX Scan Frequency: 48Mhz.

Task Completed:

- Spyglass dft_scan_ready run for RTL level scan check.
- Analyzing the synthesis reports and fixing the flow with designers on the optimization, clock gating and timing needs.
- Scan Insertion with OPCG and XOR compressor with genus flow.
- ATPG pattern generation and coverage analysis at partition level and chip_top level using Modus.
- LEC - NEQ report analysis.
- STA timing analysis for Scan_shift, stuck_at and At_speed.
- Assertion checks for IPs and PADs.
- No_timing and SDF simulation using Xcelium.

4. **Project Name: Int-SLC (INTEL)**

A low power Server SoC have 156 partitions. Clock domains used is 32. Technology node 10nm. The Scan Fabric Structure used for SCAN. The dft architecture of the SoC comprises of implementing bottom-up EDT wrappers capsuled inside Structural Test Fabric. MAX Scan Frequency: 400Mhz.

Task Completed:

- Developed python script to analyze the connected and unconnected signal for connectivity check.
- Completed the DFT-CDC report analysis and bedbug for 48 partitions and SoC level.
- Analyzing the synthesis reports and fixing the flow with designers on the optimization, clock gating, timing needs.
- Coverage Analysis at partition level.
- ATPG pattern generation and simulation at partition

level.

- Mentored and guided the engineers for DfT implementation across scan insertion, ATPG, MBIST and GLS.

5. **Project Name: Desktop SoC (INTEL)**

A low power companion SoC to augment AI platform with innovative computer vision applications. This SoC is a secure subsystem to provide a robust solution that guarantees end-user privacy. The design has 12 physical tiles/partitions with 356 memory instances and 20 clock domains. The dft architecture of the SoC comprises of implementing bottom-up EDT wrappers capsuled inside scan subsystem with OCC. The MBIST architecture to address the memory controllers based on the placement and clock domains which lead to have 45 controllers. Boundary Scan has been implemented for the SoC to integrate 1149.1 compliant elements on the SoC which have 39 pins on the chain. Technology: 28nm. MAX Scan Frequency: 25Mhz.

Task Completed:

- Developing a bottom-up synthesis flow with DC.
- Developing synthesis scripts and sdc developments.
- Analyzing the synthesis reports and fixing the flow with designers on the optimization, clock gating, timing needs.
- Defining scan architecture and strategizing the clock tree for SCAN & MBIST.
- Developing Lint flow for the partitions and SoC for the target of DfT, CDC with spyglass.
- SCAN insertion and LEC report analysis for the partitions & SoC.
- STA constraints for SCAN Shift/Capture.

6. **Design of Unified Adder Subtractor based SQRT CSLA**

Adder Subtractor

Unified Adder Subtractor (UAS) is the combination of Full Adder (FA) and Full Subtractor (FS). Its data-path element input operands are A and B, carry-in (C_{in}) and borrow-in (B_{in}) whose generated outputs are sum, carry, difference and borrow simultaneously. Each UAS unit is designed using only three XOR gate and two 2:1 MUX. In UAS design logic gates used are less (three) compared to normal FA and FS logic circuit. In this project the UAS unit is used for the design of Square-root Carry SeLect Adder (SQRT CSLA). The FA and FS unit with carry_in ='1' & Borrow_in ='1' and carry_in ='0' & Borrow_in ='0' are replaced by UAS with carry_in ='1' & Borrow_in ='1' and carry_in ='0' & Borrow_in ='0'. The UAS SQRT CSLA consume less area and power compared with BEC SQRT CSLA Adder/Subtractor. The UAS SQRT CSLA are used in the design of parallel FIR filter, MCM, and FFT where the same signals added and subtract simultaneously. The Cadence RC tools are used for area and power analysis and the Verilog HDL language used for the design.

7. Design of Even Symmetric and Odd Symmetric Parallel Fast FIR filters

The symmetric coefficient property in the parallel FIR filter is used to reduce the number of multipliers into half in the subfilter design. The multipliers and adders are huge area and power consuming datapath element in the parallel FIR filters. The pipeline and parallel processing are the two-technique used to reduce the latency and power consumption of system design, which are used in the parallel FIR filter design to increase the throughput and reduce the power consumption. The area consumption of the parallel FIR increases depend on the number of parallel block. In this project the Hcub Multiple Constant Multiplication (MCM) based multiplier and BEC SQRT CSLA adder and subtractor are used to reduce the area and power consumption. The Hcub MCM are designed by using adder, subtractor and shifter, the redundancy between the coefficients are

used to reduce the adders, subtractors and shifters by using Hcub technique. The Cadence RC Tool used for area and power analysis and Verilog HDL language used for design.

8. **Design of Reconfigurable ESPFFIR filter using VHBCSE Based MCM**

The coefficient of FIR filter can be changed dynamically at run time, this is known as Reconfigurable FIR (RFIR) filter. The Even Symmetric Parallel Fast FIR (ESPFFIR) filters in multipliers are designed by using reconfigurable Vertical Horizontal Binary Common Subexpression Elimination (VHBCSE) method to reduce the number of adder in the design of RMCM. The HCSE utilizes horizontal subexpressions (HSs) that occur within the coefficient to eliminate redundant computations and the vertical subexpressions (VSs) that occur between the adjacent coefficients are eliminated by VCSE. The Cadence RC Tool used for area and power analysis and Verilog HDL language used for design. The resource utilization in various FPGAs are analyzed using Xilinx ISE EDA tool.

JOURNAL DETAILS

- C Sheeja Herobin Rani, **R Solomon Roach**, T S Arun Samuel & S. Edwin Lawrence " Performance Analysis of Heterojunction and Hetero Dielectric Triple Material Double Gate TFET ", Silicon –Springer, Sep - 2021.

- C Sheeja Herobin Rani, K. Bhoopathy Bagan, and **R Solomon Roach** "Improved Drain Current Characteristics of Germanium Source Triple Material Double in Electrode Thickness Gate Hetero-Dielectric Stacked TFET for Low Power Applications ", Silicon –Springer, Jun-2020.

- C Sheeja Herobin Rani, K. Bhoopathy Bagan, D. Nirmal, and **R. Solomon Roach** "Enhancement of Performance in TFET by

Reducing High-K Dielectric Length and Drain Electrode Thickness", Silicon –Springer, Dec-2019.

- **R. Solomon Roach**, B Ashok, G Bhanu Teja, Ch Hemanth, C Sai Maharashi "FPGA Implementation and Power Analysis of 2-Parallel UAS based ESPFFIR filter", International Journal of Emerging Technologies and Innovative Research, ISSN:2349-5162, Vol.6, Issue 4, page no.237-241, April-2019.

- **R. Solomon Roach**, V.Adbhuta Teja, Sk.Hafheez Bhanu, Sk. Syfunnisa, V.Sreelekha "Resource and Power Analysis of CSD-VHBCSE based Reconfigurable FIR Filter on Various FPGA's", International Journal of Emerging Technologies and Innovative Research, ISSN:2349-5162, Vol.6, Issue 4, page no. pp242-250, April-2019.

- **R. Solomon Roach**, N. Nirmal Singh, T. S. Arun Samuel "Resource minimization and power reduction of ESPFFIR filter using unified adder/subtractor" Published-online Analog Integrated Circuits and Signal Processing., DOI: 10.1007/s10470-018-1284-4, year Aug 2018.

- **R. Solomon Roach**, N. Nirmal Singh, "Design of low power and area efficient ESPFFIR filter using Multiple Constant Multiplier ", Rev. Téc. Ing. Univ. Zulia. , vol. 39, no. 6, pp. 225 - 236, 2016.

- **R. Solomon Roach**, N. Nirmal Singh, C. Sheeja Herobin Rani, "Reconfigurable low power and area efficient ESPFFIR filter using VHBCSE multiplier", Journal of Advances in Chemistry, vol. 12, no. 26, pp. 5763-5769, 2016.

- A Justin Diraviam, P Loganthurai, **R. Solomon Roach** & G Angel, "Electrical Energy Monitoring Apparatus and a Method for Operating the same" Patent has been filed and published on official Journal of the Patent

Office,Issue.No.15/2018, dated 13/4/2018 page No.13354-13416.

- S.Immanuel Prabu , K.Murugan **, R.Solomon Roach,** " VLSI Based High Speed Parallel FIR Filter Design, International Journal of Emerging Technology and Advanced Engineering ISSN 2250-2459,ISO 9001:2008 Certified Journal, Volume 3, no.4, April 2013.

- A J Diraviam, SP Victor, **R Solomon Roach** & R Rajappan, " Analysis and VLSI Implementation of DIP Based Control and Monitoring of Various Physical Parameters in Process Industry" European Journal of Scientific Research, ISSN 1450-216X Vol.76 No.1 (2012), PP. 45-62.

INTERNATIONAL/NATIONAL LEVEL CONFERENCE DETAIL

- R Sriram**, R Solomon Roach** "An Energy Efficient and High Throughput TURBO Decoder Architecture" in the International conference on Emerging Technology Trends in Electrical Science organized by The Indian Engineering College, Vadakangulam, Tamilnadu, India during 27th & 28th March 2014.
- L Arivalazgan, **R Solomon Roach,** "Time Delay and Power Attenuation Method for Passive Localization of Underwater Moving Sound Sources" in the National conference on Communication, Information & Control Systems organized by VV College of Engineering, Tisaiyanvilai, Tamilnadu, India 10th April 2014.
- R. Jeni, T. Selvin Retna Raj, **R. Solomon Roach**, "Design of High performance folded DIF FFT Architecture Using MMCM Approach With Hcub Algorithm" in the International Conference on Circuit, Power and Computing Technology organized by IEEE & Noorul Islam University, Nagercoil,

Tamilnadu, India during 20st & 21nd March 2013.

- Prasanth & **R. Solomon Roach,** "Area And Power Efficient Parallel FIR Filter Using Modified Adder/Subtractor" in the 2nd International conference on Computing and Communication Technology organized by Immanuel Arasar JJ College of Engineering, Nattalam, Tamilnadu, India during 1st & 2nd March 2013.
- Vengadesh **& R.Solomon Roach,** "Design Of Low Power And Low Area Adder/Subtractor Using BEC" 2nd International conference on Computing and Communication Technology organized by Immanuel Arasar JJ College Of Engineering, Nattalam, Tamilnadu, India during 1st & 2nd March 2013.
- Vidhya & **R.Solomon Roach,** "Design of Low Power BCH Decoder Using CGFM's By Clock Gating Technique" in the 2nd International conference on Emerging Technology Trends in Advanced Engineering Research organized by Baselious Mathews II College of Engineering, Sasthamcotta, Kerala, India during 20th & 21th Feb 2012.
- Gandi & **R.Solomon Roach,** "Lifting Based 1D DWT Dataflow graph for JPEG 2000" in the national conference on MINDSS organized by Muthayammal Engineering College, Rasipuram,Tamilnadu,India during 9th & 10th April 2009.
- **R.Solomon Roach, "**Analysis of Low Power High Throughput FIR Filter Using Different Algorithm" in the national conference on RAIN'08 organized by Noorul Islam College of Engineering, Kumaracoil, Tamilnadu, India during 15th to 17th October 2008.
- A. Dyana & **R. Solomon Roach, "**Implementation of High Throughput & Low Power FIR Filter in FPGA" in the national conference on VLSI for Communication, Computation & Control organized by Karunya University, Coimbatore, Tamilnadu, India during 15th March 2008.

REVIEWER DETAIL

- **Reviewer** "International Journal of Electronics and Communications – Elsevier" .
- **Reviewer** "Analog Integrated Circuits and Signal Processing - Springer".
- **Reviewer** "International Journal of Applied Science".

SEMINAR & FACULTY DEVELOPMENT PROGRAMS DETAIL

- International Seminar in "**Embedded Platform and Design Tools"** conducted by VI Micro System, Chennai, Tamilnadu, India during 10th and 11th April, 2008.
- National Seminar in "**Emerging Trends in VLSI devices using Embedded Systems"** conducted in Noorul Islam College of Engineering, Kumaracoil, Tamil Nadu, India during 5th to 7th Oct 2007.
- Faculty Development Program on **"Networking Lab and Protocols"** conducted at Francis Xavier Engineering College, Tirunelveli, Tamilnadu, India on 25th Oct 2006.

SHORT TERM COURSES & WORKSHOPS

- Workshop on **"VLSI In Network Security"** at Cape Institute of Technology, Tirunelveli, Tamilnadu, India during 21st and 22nd Nov 2013.
- Short Term course on **"Advances in VLSI Signal Processing"** at IIT Kharagpur, India during 20th to 24th Dec 2012.
- Workshop on **"Introduction to Research Methodologies"** conducted by IIT Bombay at Cape Institute of Technology ,India during 25th June to 4th July,2012.
- **ARM Processor based Embedded System Design** at National Engineering College, Kovilpatti during 13th and 14th Aug 2008.

RESPONSIBILITIES UNDERTAKEN

- Monitoring and Reviewing the reports of 15 engineerir working for the clients like AMD, Xilinx, Rambus, Broadcom Intel, EnSilica & Qaclcomm every week.
- Doing performance review of 42 engineers in every 6 months for salary revision and bonus.
- Interviewing the fresh & experienced DfT engineers and the new trainees in recruiting process to strengthen the DfT team of Tessolve.
- Organized a 3 days workshop titled " Test & Verification o SoCs " on 9th to 11th Oct-2019 in association with Chenna Institute of Technology, Chennai.
- Training a batch of 20 intern in DfT Basic, Scan, ATPG & MBIST.
- Organized **"IoT"** workshop for the final year students in the year 2018.
- In-association with **IEEE ADSAF SIGHT** undertaken various projects for the betterment of fisherman society.
- Organized **"Science to Engineering"** electronics kit program in association with EDS chapter Coimbatore in various schools.
- To enhance the technical knowledge of the students **Electronics for You** magazine subscription was arranged for individual students.
- Organized short term courses in **Arudino** for 2nd, 3rd and fina year students**.**
- Set up **"Texas Instrumentation Innovation lab"** in Cape Institute of Technology during the year 2016**.**
- **Coordinator** of **IEEE student Branch** Cape Institute o Technology from 2014.
- **Organized** a Inter College Paper Contest on**" E-Waste"** or 13th March 2015 in association with IEEE Student Branch Cape Institute of Technology, Levengipuram.
- **Co-Convener** for two day workshop on **Image Processing HDL co-simulator using System Generator"** in Cape Institute of Technology, Tirunelveli on 30th & 31st Nov 2014.
- **Project guide** for UG & PG students of Cape Institute o Technology, Tirunelveli for 4 years.
- **Co-Convener** for two day workshop on **VLSI in Network Security** at Cape Institute of Technology, Tirunelveli on 21st & 22nd Nov 2013.
- **Chairing the session** - VLSI papers in **2011 IEEE International Conference on Computational Intelligence and Computing Research** at Cape Institute of Technology held during 15th to 18th Dec 2011.
- **Project co-ordinator** for M.E - VLSI students in Francis

Xavier Engineering College, Tirunelveli in the year 2008-2009.

- **Co-ordinator** for two day workshop on **Labview Software and hardware** conducted by Reach Information and communication systems, Coimbatore in Francis Xavier Engineering College, Tirunelveli.